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What is claimed is:

1. An automated method for designing an initial integrated circuit layout with a computer, based upon an electronic circuit description and by using a cell library containing cells that each have an associated relative delay value, comprising the steps of:

(a) selecting a plurality of cells from the cell library that are intended to be coupled to each other with a plurality of wires and that can be used to implement the digital circuit based on the electronic circuit description input to the computer; and

(b) determining, using a portion of a computer program that contains a sequence of instructions, an initial intended area of each of the selected plurality of cells, the initial intended area of at least some of the selected plurality of cells being determined using the associated relative delay value of the selected cell and the initial intended lengths of some of the wires coupled to each of said some cells in order to meet predetermined

timing constraints associated with each of said some cells that are coupled to another cell.

2. The automated method of claim 1 further comprising:

routing the digital circuit to generate the integrated circuit layout using the finalized area of each of the selected plurality of cells and the finalized wire lengths.

3. The automated method of claim 2 further comprising:

prior to the step of routing, finalizing the area of each of the selected plurality of cells and the lengths of the wires.

4. The method of claim 1 wherein the plurality of cells are coupled to each other based on the electronic circuit description input to the computer.

5. The automated method of claim 1 wherein each of the plurality of wires has an associated capacitive load value; and

wherein each wire is associated with a net weight value that represents the sensitivity of the total area of the digital circuit of step (a) with respect to the associated capacitive load value of the wire.

6. The automated method of claim 5 wherein the net weight w_i of the wire coupled to a selected cell is:

$$w_i = \partial A / \partial C_i$$

where A is the total area of the digital circuit of step (a) and C_i is the associated capacitive load of the wire coupled to the selected cell.

7. The automated method of claim 6 wherein the initial intended areas of said some selected cells are chosen based upon the net load w_i in order to meet said predetermined timing constraints.

8. The automated method of claim 1 wherein the initial intended areas of said some selected cells are chosen based upon the length of said some wires coupled to said some selected cell.

9. The automated method of claim 6 wherein the initial intended areas of said some selected cells are chosen based upon the net load w_i of the wires coupled to said some selected cells and the lengths of the wires coupled to said some selected cells.

10. The automated method of claim 1 further comprising:

inserting a buffer in one of the wires of step (a) to reduce an area of a cell coupled to the wire.

11. The automated method of claim 10 wherein the step of inserting the buffer comprises:

determining a wire in the digital circuit of step (a) into which a buffer can be inserted to

reduce an area of a cell coupled to the wire by a specific area size; and

inserting the buffer into the wire if an area of the buffer is less than the specific area size, prior to the step (b) of determining the initial intended area of each of the selected plurality of cells.

12. The automated method of claim 1 further comprising:

stretching the associated relative delay value of a selected cell to decrease the area of the selected cell.

13. The automated method of claim 1 further comprising:

stretching the associated relative delay values of a plurality of selected cells coupled to each other to decrease the area of each of the coupled cells.

14. The automated method of claim 1 further comprising:

compressing the associated relative delay value of a selected cell to assist in satisfying the predetermined timing constraints.

15. The automated method of claim 14 wherein the compressing step is limited by a gain requirement of the selected cell.

16. The automated method of claim 1 further comprising:

compressing the associated relative delay values of a plurality of the selected cells to assist in satisfying the predetermined timing constraints.

17. The automated method of claim 1 wherein a group of said some cells are assigned in buckets and operated upon in order to determined the initial intended area of each of the group of said some cells.

18. The automated method of claim 17 wherein the group of said some cells ranges from 20 to 200 cells.

19. An integrated circuit layout produced in accordance with the automated method of claim 1.

20. An automated method for designing an integrated circuit layout using a computer, based upon an electronic circuit description and based upon cells which are selected from a cell library, each of the cells having an associated area, comprising the steps of:

(a) placing each of the cells in the integrated circuit layout so that the cells can be coupled together by wires to form a circuit path having an associated predetermined delay constraint wherein the cells are coupled together by wires based upon the electronic circuit description input to the computer; and

(b) adjusting an area of at least one of the cells to satisfy the associated predetermined delay constraint of the circuit path.

21. The automated method of claim 20 wherein each of the wires has an associated capacitive load value; and

wherein each wire is associated with a net weight value that represents the sensitivity of the total area of the integrated circuit layout with respect to the associated capacitive load value of the wire.

22. The automated method of claim 21 wherein the net weight w_i of the wire coupled to a cell is:

$$w_i = \partial A / \partial C_i$$

where A is the total area of the integrated circuit layout and C_i is the associated capacitive load of the wire coupled to the cell.

23. The automated method of claim 22 wherein the

areas of at least some of the cells are chosen based upon the net load w_i in order to meet said predetermined timing constraints.

24. The automated method of claim 20 wherein the areas of said some cells are chosen based upon the lengths of at least some of the wires coupled to said some cells.

25. The automated method of claim 22 wherein the areas of said some selected cells are chosen based upon the net load w_i of the wires coupled to said some selected cells and the lengths of the wires coupled to said some selected cells.

26. The automated method of claim 20 further comprising:

inserting a buffer in one of the wires of step (a) to reduce an area of a cell coupled to the wire.

27. The automated method of claim 20 further

comprising:

stretching the associated relative delay value of a selected cell to decrease the area of the selected cell.

28. The automated method of claim 20 further comprising:

compressing the associated relative delay value of a selected cell to assist in satisfying the predetermined timing constraints.

29. The automated method of claim 28 wherein the compressing step is limited by a gain requirement of the selected cell.

30. The automated method of claim 20 wherein a group of said some cells are assigned in buckets and operated upon in order to determined the initial intended area of each of the group of said some cells.

31. The automated method of claim 30 wherein the group of said some cells ranges from 20 to 200 cells.

32. An integrated circuit layout produced in accordance with the automated method of claim 20.

33. An automated method for designing an integrated circuit layout of at least four cells by using a computer and based upon an electronic circuit description containing information on the digital circuit, comprising the steps of:

(a) selecting a plurality of cells which can be used to implement the digital circuit based upon the electronic circuit description, each of the plurality of cells having an associated load, the plurality of cells comprising a first cell having a first load, a second cell having a second load, a third cell having a third load, and a fourth cell having a fourth load, each of the cells and the associated load having a predetermined associated delay value;

(b) determining initial placement locations for each of the selected plurality of cells including the first cell, the second cell, the third cell, and the fourth cell;

(c) setting the size of each of the selected plurality of cells and the loads of each cell so that the predetermined associated delay value of at least some of the selected plurality of cells with associated loads remain relatively constant; and

(d) routing the digital circuit based on the finalized location and size of each of the selected plurality of cells.

34. The automated method of claim 33 wherein each of the load has an associated capacitive load value; and

wherein each load is associated with a net weight value that represents the sensitivity of the total area of the integrated circuit layout with respect to the associated capacitive load value of the load.

35. The automated method of claim 34 wherein the net weight w_i of the load coupled to a cell is:

$$w_i = \partial A / \partial C_i$$

where A is the total area of the integrated circuit layout and C_i is the associated capacitive load of the load coupled to the cell.

36. The automated method of claim 35 wherein the areas of at least some of the cells are chosen based upon the net load w_i in order to meet said predetermined timing constraints.

37. The automated method of claim 33 wherein the areas of said some cells are chosen based upon the lengths of at least some of the wires coupled to said some cells.

38. The automated method of claim 36 wherein the areas of said some selected cells are chosen based upon the net load w_i of the loads coupled to said some selected cells and the lengths of the loads coupled to said some selected cells.

39. An integrated circuit layout produced in accordance with the automated method of claim 32.

40. An automated method for determining an integrated circuit layout of at least four cells by using a computer and based upon an electronic circuit description containing information on the digital circuit, the automated method comprising the steps of:

(a) selecting a plurality of cells which can be used to implement the digital circuit using the electronic circuit description, the plurality of cells each comprising a first cell having a first load and a first predetermined timing constraint, a second cell connected to the first cell and having a second load and a second predetermined timing constraint, a third cell connected to the second cell and having a third load and a third predetermined timing constraint, and a fourth cell connected to the third cell and having a fourth load and a fourth predetermined timing constraint;

(b) determining the placement locations for each of the selected plurality of cells including the first cell, the second cell, the third cell, and the fourth cell;

(c) selecting the size of the first cell based on the first load of the first cell and on the first predetermined timing constraint;

(d) selecting the size of the second cell based on the second load of the second cell and on the first predetermined timing constraint and the second predetermined timing constraint;

(e) selecting the size of the third cell based on the third load and on the first predetermined timing constraint, the second predetermined timing constraint and the third predetermined timing constraint;

(f) selecting the size of the fourth cell based on the fourth load and on the first predetermined timing constraint, the second predetermined timing constraint, the third predetermined timing constraint, and the fourth predetermined timing constraint;

(g) routing the digital circuit based on the placement location and size of each of the selected plurality of cells.

41. An integrated circuit layout produced in accordance with the automated method of claim 40.